Directional and Single-Driver Wires in FPGA Interconnect

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Professor Lemieux and his students have had a long-established record of contributing ideas related to FPGA architecture with an emphasis on efficient resource usage and performance. A common theme throughout his research has been the efficiencies of interconnection strategies (or interconnect) and communication across a chip.

The 2004 paper, "Directional and Single-Driver Wires in FPGA Interconnect" inspired the community to reexamine a basic assumption on programmable interconnect within an FPGA. Programmable wires within an FPGA are relatively expensive relative to non-programmable interconnect and even programmable logic. As the number of metal layers in integrated circuits increased over the years, the programmable wire cost formulation needed to be reexamined.

Professor Lemieux, Edmund Lee, Marvin Tom, and Anthony Yu clearly articulated and quantified the gains associated with adopting programmable interconnect strategies within the core of a given FPGA architecture. This paper has been cited by many research teams seeking to build upon interconnect efficiencies and contribute further towards FPGA architectures.

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