A high−performance microarchitecture with hardware−programmable functional units

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Two of the most important research problems in FPGA computing have been automating FPGA computing for the software developer, and coupling the FPGA compute fabric to its host computer. This 25-year-old paper did an elegant and effective job of addressing both.

Their PRISC (PRogrammable Instruction Set Computer) has a three-level array of combinational LUTs and configurable interconnect as a Programmable Functional Unit (PFU) in the heart of a RISC CPU, alongside its ALU. You can't couple an FPGA fabric any closer to its host; the host-FPGA latency is essentially zero. This PFU takes less area than a 1 KB SRAM.

The PRISC compiler automatically analyzes C programs for opportunities to implement application-specific custom operations in the PFU. It has a hardware detection phase, which identifies operations that are good candidates for PFU implementation, and walks the control-flow graph seeking to combine these operations into a single PFU expression. Then the compiler uses its hardware synthesis phase (possibly the first logic synthesis component in a software compiler) to compile the PFU expression into LUTs and interconnect. All such opportunities are found and compiled into PFU configurations, which are loaded into PFU hardware at runtime by custom instructions. Thus the task of identifying speedup opportunities and compiling them into FPGA form is completely automated.

Performance modeling of the PRISC compiler and CPU showed 22% speedup on the SPECint92 benchmarks, which is impressive for such ease of use and minimal area overhead at this early date. The authors wisely limited the scope of their work to combinational functions of two inputs, in a simple in-order CPU microarchitecture, leaving the problems of managing PFU state, richer functions and superscalar processors as opportunities for further research.

PRISC had a profound influence on this field; ACM lists 117 citations. Probably the strongest impact was on the technology developed and deployed by the team at Stretch Technologies, in their software-configurable processor families. They combined an FPGA fabric with a high-performance RISC CPU, augmented by a 128-bit register file and 128-bit path to memory directly connected to the fabric. Its C/C++ compilation process produced FPGA-optimized instructions and machine code, and configured the FPGA fabric, automatically. Silicon and software was deployed into camera and broadcast video processing and wireless applications. Stretch was acquired by Exar in 2014.

Automating FPGA computing and coupling the FPGA fabric to its host remain major active areas of research today. PRISC helped get these efforts off to a solid start.

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