A User Programmable Reconfigurable Logic Array

William S. Carter, Khue Duong, Ross H. Freeman, Hung-Cheng Hsieh, Jason Y. Ja, John E. Mahoney, Luan T. Ngo and Shelly L. Sze

Published: *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC), May 1986, pp. 233--235.*

This paper describes the Xilinx' first product, the 2000 series FPGA architecture and the first device built with it, containing many FPGA "firsts" in just a one and half page paper! It was the first paper describing a commercial programmable logic device (PLD) that employed a 2-dimensional array architecture (just like the fabricated gate arrays of the time) of logic surrounded by routing. It is also the first commercial PLD that employed static RAM memory-based programming technology, when all previous devices were either fused, EPROM or EEPROM-based. The static RAM programmability gave rise to the idea of rapid change of the functionality, leading to the possibility of "dynamic hardware" as the authors call it, which is in use broadly today.

The paper also gives a first report of programmable function generator-as-logic-element that turns out to be a lookup table (LUT) that has since become ubiquitous in the industry. The programmable interconnect method was also novel---using a chain of connected NMOS pass transistors to get from drivers to syncs, rather than full or partial crossbars then extant in PLDs. That NMOS pass transistor survives in a different form today; even back then Carter et. al. noted the need for 'bidirectional repeaters' to compensate for reduced signal quality.

The description of the essential functionality of the device reveals the state of the art of the time: a 2μm CMOS process, just 64 logic blocks and 58 I/O blocks.   There is *no mention* of the software tools need to configure the device, which were strictly manual at the time!

One interesting note, not obvious in the paper but true of the Xilinx 2000 (and 3000) series architecture: it employed what was essentially a fracturable 4-input lookup table (being usable as two three-input lookup tables with some input sharing) indicating the architects' intuition around the value of flexibility and the importance of making use of the expensive programmable connections. Fracturability went out of fashion, but returned later (in the early 2000s) in the face of research that showed the value that arises in a time of full logic synthesis.

This paper described many of the unique aspects of the core capability and functionality of FPGAs and was a harbinger of the dynamic and enabling industry to come.

 Endorsement by: Jonathan Rose, Professor, University of Toronto