# An Efficient Logic Emulation System

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There is always "that" paper, the one you keep coming back to, learning more from; the one that seemed simple at the beginning, but ended up moving industries, spawning lawsuits, and changing the world, or at least some portion of it. This paper, which really is a short teaser of the magnificent US Patent 5,036,473, is "that paper" for logic emulation, and reconfigurable computing more generally.

From the earliest days of FPGAs, it was clear that there was something special about these devices that simply must lead to a revolution to how computation was done. Many companies tried, and researchers developed systems, but the promise often was left unfulfilled, with the reconfigurable computing community wondering what the "killer app" for these systems would be.

This paper was an answer---take a large number of FPGAs, hooked up in an efficient interconnect structure, and use it as a high-speed simulation fabric for VLSI chip designs. This was the birth of logic emulation. By providing a local crossbar to communicate between individual FPGAs, and a hierarchy of ever-higher levels of crossbar to hook up boards, systems, and chassis together, this essentially welds the small-capacity devices of any era into a supercomputer installation able to support even the most complex digital designs.

Although others (including myself in my own Ph.D. research) might scoff at the notion of wasting so many devices on mere interconnect, in hindsight the authors were exactly right---wiring is the problem, and efficient use of reconfigurable logic for routing in a crossbar was the answer.

Since that time logic emulation has become a battleground of companies building upon this foundation, creating machines, and an industry, that is indispensable for the development of microprocessor and other bleeding-edge digital chips. And as for the paper, and the patent behind it? Well, 25 years later I still find myself teaching the material, and returning to them repeatedly to learn new things.

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