FlowMap: An Optimal Technology Mapping Algorithm for Delay Optimization in Lookup-Table Based FPGA Designs

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This paper represents pioneering work in the area of technology mapping for FPGAs and presents a theoretical breakthrough by solving the LUT-based FPGA technology mapping problem for depth minimization optimally in polynomial time. The key idea was to model the LUT mapping problem as the computation of a minimum-height, K-feasible cut. This was the first global formulation of the LUT mapping problem, since other mapping algorithms at the time were based on local clustering and could not guarantee optimality. Another key contribution of the paper was to exploit the flexibility of LUTs in an FPGA, making the FPGA mapping problem easier compared to ASIC technology mappers, by only structurally considering the number of inputs to a subgraph.

The new network-flow-based algorithm presented in this paper showed excellent results on depth optimization as well as a significant reduction in the number of LUTs used, when compared to all previous methods. This is an important result because it has a direct correlation to the size of designs that can be fit into FPGAs. Having fewer LUTs increases the design size that can be mapped and fitted onto the FPGA. Depth minimization also has a direct correlation to improving the timing performance of the design, while trading off area since the algorithm computes each cut independently which could result in implicit logic duplication.

While FPGA technology mapping has evolved since this paper was published, this paper laid the theoretical foundation for many technology mapping implementations that are very key to the FPGA industry today. Several subsequent technology mapping papers have also used the theoretical framework of FlowMap and refined the approach to optimize for multiple objectives simultaneously.

This paper also serves as a great reference material and tutorial for students and industry professionals who are interested in learning about FPGA technology mapping and FPGA design implementation.

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